Abstracts

Simulating "Large" Microwave Circuits with the Parallel Planar Generalized Yee Algorithm

S. Gedney, F. Lansing, R.T. Kihm, N. Owona and K. Virga. "Simulating "Large" Microwave Circuits with the Parallel Planar Generalized Yee Algorithm." 1996 MTT-S International Microwave Symposium Digest 96.2 (1996 Vol. II [MWSYM]): 1011-1014.

The Planar Generalized Yee (PGY) algorithm is presented for the full-wave analysis of "electrically-large" grounded co-planar (GCPW) circuits. The method has a significant advantage over traditional Yee-algorithm based finite-difference time domain (FDTD) methods in that it is based upon unstructured and irregular grids. The PGY algorithm has been efficiently implemented on massively parallel computers and is ideal for the rapid, broadband analysis of packaged, large, high-density circuits and multi-chip modules (MCM's). Simulation and measured results on several "electrically-large" circuit structures are presented.

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